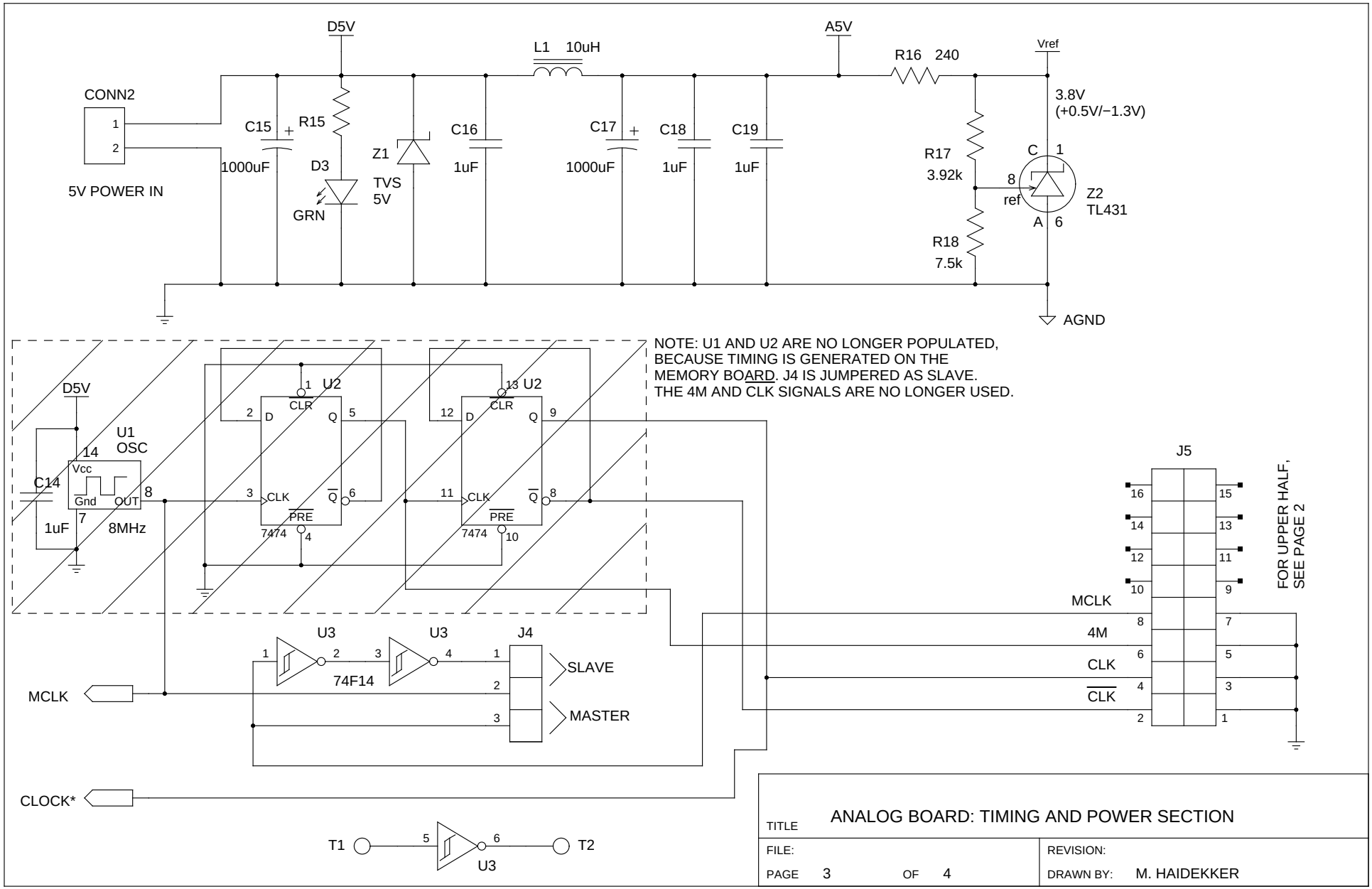
D5V
A5V
Vref
L1 10uH
R16 240
CONN2
1
2
5V POWER IN
C15
1000uF
R15
D3
GRN
Z1
TVS
5V
C16
1uF
C17
1000uF
C18
1uF
C19
1uF
R17
3.92k
R18
7.5k
3.8V
(+0.5V/−1.3V)
C 1
8
ref
A 6
Z2
TL431
AGND
NOTE: U1 AND U2 ARE NO LONGER POPULATED,
BECAUSE TIMING IS GENERATED ON THE
MEMORY BOARD. J4 IS JUMPERED AS SLAVE.
THE 4M AND CLK SIGNALS ARE NO LONGER USED.
D5V
U1
OSC
14
Vcc
Gnd
OUT
8
7
C14
1uF
8MHz
U2
1 CLR
2 D
Q 5
3 CLK
Q 6
PRE
7474
4
U2
13 CLR
12 D
Q 9
11 CLK
Q 8
PRE
7474
10
J5
16
15
14
13
12
11
10
9
MCLK
8
7
4M
6
5
CLK
4
3
CLK
2
1
FOR UPPER HALF,
SEE PAGE 2
U3
1
2
74F14
U3
3
4
J4
1
2
3
SLAVE
MASTER
MCLK
CLOCK*
T1
5
6
U3
T2
TITLE
ANALOG BOARD: TIMING AND POWER SECTION
FILE:
REVISION:
PAGE 3 OF 4
DRAWN BY: M. HAIDEKKER